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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/792,257	03/02/2004	Aaron J. Steyskal	884.B85US1	4001

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EXAMINER	
HA, NGUYEN T	

ART UNIT	PAPER NUMBER
2831	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/792,257	STEYSKAL ET AL.	
	Examiner	Art Unit	
	Nguyen T Ha	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *6-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 18-21* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-5 and 18-21 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, and 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over DuPre' et al. (US 5,880,925) in view of Greenwood et al. (US 6,751,087).

Regarding claim 1, DuPre' et al. disclose a capacitor (figure 1) comprising:

- a capacitor package/capacitor body (42 column 5, line 18);
- a number of plate assemblies (58 & 60) housed within the capacitor package (42), each plate assembly having a first polarity connection (44, column 5, line 19) and second polarity connections (46, column 5, line 20); and

DuPre' et al. lacks a plurality of terminals, wherein multiple first polarity connections are coupled to a single first polarity terminal and corresponding multiple second polarity connections are coupled to multiple second polarity terminals.

Greenwood et al. teach a plurality of terminals (figures 1 and 3a-3b), wherein multiple first polarity connections (101) are coupled to a single first polarity terminal and corresponding multiple second polarity connections (102) are coupled to multiple second polarity terminals (figures 1 and 3a-3b).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the assembly of Greenwood et al. in DuPre' et al. in order to increase surface area for the capacitor.

Regarding claim 3, DuPre' et al. disclose the plurality of terminals including at least one surface mount terminal (column 5, lines 34-41).

Regarding claim 5, DuPre' et al. disclose the capacitor package including a rectangular volume (column 2, lines 17-26).

Regarding claim 4, DuPre' et al. disclose all the claimed limitations discussed above with respect to claim 1, except for the first polarity is an anode and the second polarity is a cathode. It would have been obvious to one having ordinary skill in the art at

the time invention was made to have a first polarity is an anode and a second polarity is a cathode, since it was known in the art that the capacitor should have the positive and negative sides.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over DuPre' et al. (US 5,880,925) in view of Greenwood et al. (US 6,751,087) as applied in claim 1 above, and further in view of Nitoh (US 6,421,227).

Regarding claim 2, the teaching of DuPre' in view of Greenwood et al. disclose all the claimed limitations with respect to claim 1 above, except for the number of plate assemblies including a number of fan-like assemblies.

Nitoh et al. teach, at column 7, lines 5-22, forming a plate assembly having an unfolded fan-like shape (fig 1) in order to prevent the concentration of stress when the plates are stacked. Moreover, Nitoh et al. teach that having such an assembly provides an easier means of stacking and fixing. As a result, a multilayer capacitor element having an excellent heat resistant property is achieved.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the plate assemblies of DuPre et al. in view of Greenwood et al. in a fan-like shape in view of the teaching of Nitoh et al. in order to prevent the concentration of stress when the plates are stacked.

5. Claims 18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda et al. (US 6,351,369) in view of DuPre' et al. (US 5,880,925) and Greenwood et al. (US 6,751,087).

Regarding claim 18, Kuroda et al. prior art disclose an information handling system (figure 8), comprising:

- a motherboard (not shown);
- a voltage regulation circuit (2) coupled to the motherboard, including a capacitor (5) that includes:
- a processor chip (3);
- a dynamic random access memory (4); and
- a bus (not shown) coupled between processor chip and the dynamic random access memory (figure 8).

Kuroda et al. lack : a capacitor comprising :

- a capacitor package;
- a number of plate assemblies housed within the capacitor package, each plate assembly having a first and a second polarity connections; and
- a plurality of terminals, wherein multiple first polarity connections are coupled to a single first polarity terminal and corresponding multiple second polarity connections are coupled to multiple second polarity terminals.

The teaching of DuPre et al. in view of Greenwood et al. disclose all the missing limitations in the above with respect to claim 1.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the DuPre' et al. in view of Greenwood et al. capacitor into

Kuroda et al. system in order to provide an improvement surface mount compatible decoupling capacitor for use in the electronic system.

Regarding claim 21, DuPre' et al. further teach the plurality of terminals includes multiple first polarity terminals (figure 4).

6. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda et al. (US 6,351,369) in view of DuPre' et al. (US 5,880,925) and Greenwood et al. (US 6,751,087) as applied in claim 18 above, and further in view of Palanduz et al. (US 6,795,296).

Regarding claim 19, the teaching of Kuroda et al. in view of DuPre' et al. and Greenwood et al. disclose all the claimed limitations with respect to claim 18 above, except for the dynamic random access memory includes a synchronous dynamic random access memory.

Palanduz et al. disclose a memory includes a synchronous dynamic random access memory (SDRAM) (column 2, lines 50-55).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the SDRAM memory of Palanduz et al. into Kuroda in view of DuPre' and Hansen et al., in order to improve the speed for the system.

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda et al. (US 6,351,369) in view of DuPre' et al. (US 5,880,925) and Greenwood et al. (US 6,751,087) as applied in claim 18 above, and further in view of Greenwood et al. (US 6,590,762).

Regarding claim 20, the teaching of Kuroda et al. in view of DuPre' and Greenwood disclose all the claimed limitations with respect to claim 18 above, except for the capacitor package includes a cylindrical volume.

Greenwood et al (US, 6,590, 762). disclose a capacitor package includes a cylindrical volume (claim 4 and claim 11).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the cylindrical capacitor case/housing of Greenwood in Kuroda in view of DuPre and Greenwood et al., in order to facilitate for the manufacture and the user.

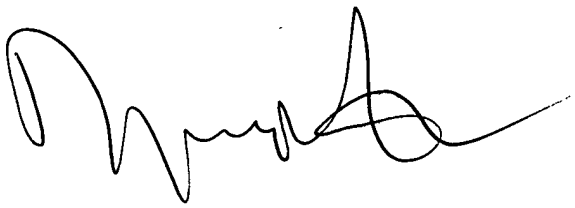
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nguyen T. Ha whose telephone number is 571-272-1974. The examiner can normally be reached on Monday-Friday from 8:30AM to 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-2800 ext. 31. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Nguyen T. Ha
October 16, 2005